In the claims:

For the Examiner's convenience, all pending claims are presented below.

1-24. (Cancelled)

25. (Previously Presented) A memory cell comprising:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor;

a first storage node coupled between the first PMOS transistor and the first NMOS transistor;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor; and

a second storage node coupled between the second PMOS transistor and the second NMOS transistor;

the first and second PMOS transistors to receive a reverse bias voltage whenever the memory cell is operating in a read mode.

26. (Previously Presented) The memory cell of claim 25 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

27. (Previously Presented) The memory cell of claim 25 wherein the first and second PMOS transistors receive a forward bias voltage whenever the memory cell is operating in a standby mode.

28. (Previously Presented) The memory cell of claim 27 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

29. (Previously Presented) A computer system comprising:

a microprocessor; and

a memory device comprising:

one or more memory cells including a N-channel component, and a P-channel component formed within the N-channel component;

a gap cell formed within the N-channel component; and

a contact within the gap cell to provide a bias control signal to the P-channel components within a memory cell.

30. (Previously Presented) The computer system of claim 29 wherein the P-channel component of each memory cell comprises:

a first PMOS transistor; and

a second PMOS transistor, the first and second PMOS transistors to receive a bias control signal.

31. (Previously Presented) The computer system of claim 30 wherein the N-channel component of each memory cell comprises:

a first NMOS transistor coupled to the first PMOS transistor; and

a second NMOS transistor coupled to the second PMOS transistor.

32. (Previously Presented) The computer system of claim 31 wherein each memory

cell further comprises:

a first storage node coupled between the first PMOS transistor and the first NMOS transistor; and

a second storage node coupled between the second PMOS transistor and the second NMOS transistor.

33. (Previously Presented) The computer system of claim 32 wherein the bias control signal delivers a forward bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a standby mode.

34. (Previously Presented) The computer system of claim 33 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

35. (Previously Presented) The computer system of claim 32 wherein the bias control signal delivers a reverse bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a read mode.

36. (Previously Presented) The computer system of claim 35 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

37. (Previously Presented) A memory cell comprising:

a first load and access transistor;

a first body transistor coupled to the first load and access transistor;

a first storage node coupled between the first load and access transistor and the first body transistor;

a second load and access transistor;

a second body transistor coupled to the second load and access transistor; and

a second storage node coupled between the second load and access transistor and the second body transistor;

the first and second load and access transistors to receive a bias control signal to deliver a forward bias voltage to the first and second load and access transistors whenever the memory cell is operating in a standby mode.

38. (Previously Presented) The memory cell of claim 37 wherein the first and second load and access transistors are PMOS transistors.

39. (Previously Presented) The memory cell of claim 38 wherein the first and second body transistors are NMOS transistors.

40. (Previously Presented) The memory cell of claim 37 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

41. (Previously Presented) The memory cell of claim 37 wherein the bias control signal delivers a reverse bias voltage to the first and second load and access transistors whenever the memory cell is operating in a read mode.

42. (Previously Presented) The memory cell of claim 41 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

43. (Previously Presented) A method comprising:

a memory cell entering a standby state;

receiving a forward bias voltage at load and access transistors within the memory cell; and

maintaining a storage value at a first node within memory cell in response to receiving the forward bias voltage.

44. (Previously Presented) The method of claim 43 further comprising:

the memory cell entering a read state; and

receiving a reverse bias voltage at the load and access transistors.

45. (Previously Presented) The method of claim 43 further comprising:

the memory cell entering a read state; and

receiving a reverse bias voltage at the load and access transistors.

46. (Previously Presented) The method of claim 45 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.